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Integration of InGaAs/InP Single Photon Avalanche Diode and Thin Film Lithium Niobate Photonic Chip via Photonic Wire Bonding

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Thin-film lithium niobate (TFLN) is a powerful platform for integrated quantum photonic chips thanks to its excellent performance on high-speed optical modulation, low waveguide loss, and strong nonlinear effects. However, realizing compact and cost-effective single-photon detection on TFLN photonic chips is challenging. Photonic wire bonding (PWB) is a flexible chip-to-chip and chip-to-fiber optical interconnection technology. In this work, PWB technology is used to achieve hybrid integration of InGaAs/InP single-photon avalanche diodes (SPADs) and TFLN photonic chips. A suspended polymer waveguide with a span over 300 µm is fabricated by two-photon polymerization to connect the TFLN dual-layer coupling structure (DLCS) and the photon-sensitive area of the SPAD, through which high-performance optical coupling between the TFLN photonic chip and the SPAD is achieved. Experiments show that the integrated SPAD has an on-chip photon detection efficiency (PDE) of 13.8% at −30 °C, with a dark count rate (DCR) of 6×10^{-4} Hz/gate, an after-pulse probability (APP) of 3%, and a time jitter of 370 ps. This work shows that PWB provides a convenient solution for the hybrid integration of single-photon detectors on TFLN photonic chips, which has great potential for developing compact and low-cost on-chip systems for quantum communication, quantum information processing, and weak light sensing.

1. Introduction

Quantum photonic chips provide a stable and scalable way to develop complicated photonic quantum information systems.[1] In recent years, various material platforms have been extensively explored, including silica,[2] silicon,[3] indium phosphide (InP),[4] silicon nitride,[5] thin-film lithium niobate (TFLN),[6,7] and so on. Among these, TFLN has attracted significant attention and been used in some applications of quantum photonics, thanks to its excellent performance on low waveguide loss,[8] high-speed optical modulation,[9] and strong nonlinear effects. For instance, spontaneous parametric down-conversion (SPDC) photon-pair sources have been achieved by periodically poled lithium niobate (PPLN) waveguides on TFLN photonic chips[10] for quantum communication and imaging. High-speed optical modulation on TFLN photonic chips has been applied to realize encoding/decoding functions in quantum key distribution (QKD), which enhances the secure key rate of QKD.[11,12] On the other hand, the TFLN material could not support single photon detection, limiting its capability for on-chip quantum state measurement. Hence, hybrid or heterogeneous integration of single-photon detectors with TFLN photonic chips is required for developing TFLN-based quantum photonic chips. In this work, we focus on the integration of telecom-band single-photon detectors on TFLN photonic chips, since the high-speed optical modulation on TFLN photonic chips is preferred for applications of quantum photonics over optical fiber, such as photon-counting optical time-domain reflectometer (OTDR),[13] and QKD.[14]

Commonly used telecom-band single-photon detectors in quantum photonics include superconducting nanowire single-photon detectors (SNSPDs) and single-photon avalanche diodes (SPADs). SNSPDs have many attractive properties, including high detection efficiency, low dark counts, broad detection bandwidth, low time jitter, and so on. SNSPDs are easy to integrate on various materials, since the superconducting nanowires are thin films of several nanometers in thickness. They have been integrated on TFLN photonic chips, and the reported

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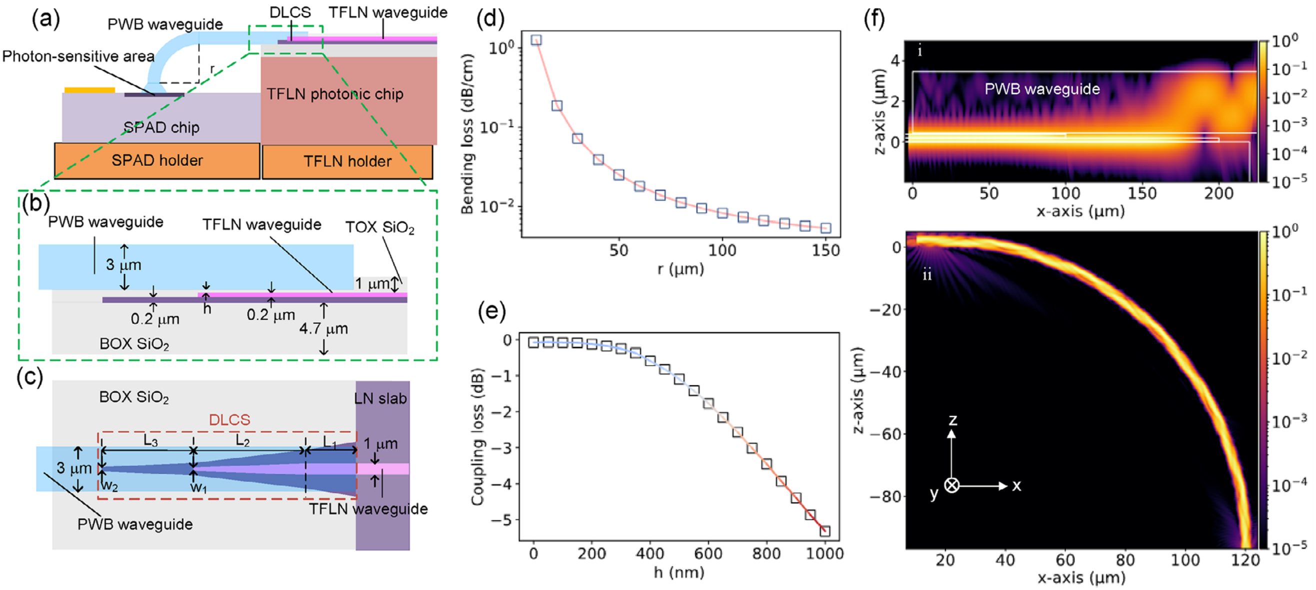

Figure 1. Scheme and simulation results of the integration of the InGaAs/InP SPAD and the TFLN photonic chip via PWB. a) Schematic illustration of hybrid integration between the TFLN photonic chip and the SPAD via PWB. b) Longitudinal profile of the TFLN waveguide, the DLCS, and the PWB waveguide, with structure parameters. c) Top view of the DLCS, including the adiabatic taper of the ridge and the multi-segment strip taper. d) Simulation result of the bending loss of the PWB waveguide under different bending radii. It shows that the bending loss would be less than 10^{-2} dB cm^{-1} under a radius > 90 μm. e) Simulation result of the coupling loss of the DLCS and the PWB waveguide under different oxide layer thickness (*h*) on the DLCS. f) Full-wave FDTD simulation of light coupling and propagation. f-(i) Adiabatic mode transformation from the TFLN waveguide to the PWB waveguide. f-(ii) Light propagation along the PWB waveguide with a 100 μm bending radius. Total insertion loss is 0.27 dB.

on-chip efficiencies are 20%–40%.[15,16] However, the operation of SNSPDs requires a cryogenic environment, limiting their practical applications in some scenarios. InGaAs/InP SPADs operate at near room temperature by thermal electronic cooler (TEC) and have been widely used in applications with optical fiber transmission. Recently, the performance of InGaAs/InP SPADs at room temperature has been highly improved, which is promising in applications requiring cost-effective and compact single-photon detectors.[17,18] Large lattice mismatch between InGaAs/InP and TFLN limits their heteroepitaxial integration. Hence, the hybrid integration method of InGaAs/InP SPADs with TFLN photonic chips is an important topic to extend the functions of TFLN-based quantum photonic chips.

Photonic wire bonding (PWB) technology, a 3D polymer waveguide fabrication method based on two-photon polymerization, provides a flexible optical interconnection solution for photonic chips,[19,20] enabling low-loss and alignment-tolerant chip-to-chip or chip-to-fiber optical coupling.[21,22] However, this technology has not been applied to chip-to-detector interconnection. It is not clear whether the high-power femtosecond laser light in the PWB fabrication process would damage detectors or not. A large-span suspended waveguide with enough mechanical stability is also a challenge for the chip-to-detector connection. Especially, as a hybrid integration technique for SPAD, it is essential to have a low-loss optical coupling between the SPAD and the TFLN photonic chip to achieve a high photon detection efficiency.

In this work, we demonstrate the hybrid integration of an InGaAs/InP SPAD and a TFLN photonic chip via PWB technology, using a piece of polymer waveguide with a suspended span over 300 μm. The photonic circuit of the TFLN chip is fabricated on a lithium niobate-on-insulator (LNOI) substrate with a top lithium niobate layer of 400 nm in thickness. A dual-layer coupling structure (DLCS) is designed and fabricated at the end of the TFLN waveguide as the interface with the polymer waveguide. Photons are guided from the TFLN waveguide to the photon-sensitive area of the SPAD via the polymer waveguide. The performance of the integrated SPAD is measured at −30 °C, achieving a maximum on-chip photon detection efficiency of 13.8%, a dark count rate of $\approx 6 \times 10^{-4}$ Hz/gate, an after-pulse probability of ≈3%, and a time jitter of ≈370 ps. This work shows that PWB provides a convenient solution for the hybrid integration of InGaAs/InP SPADs and TFLN photonic chips. The method has the potential to be extended to other types of quantum photonic chips and single-photon detectors.

2. Methods and Results

2.1. The Scheme and Simulation Results

The integration scheme of the InGaAs/InP SPAD and the TFLN photonic chip via PWB is illustrated in **Figure** 1a. Photons propagating along the TFLN waveguide are coupled into the PWB waveguide through a dual-layer coupling structure (DLCS) at the end of the TFLN waveguide. The PWB waveguide then directs the photons vertically to the photon-sensitive area of the SPAD for detection. The longitudinal profile and top view of the DLCS and the PWB waveguide are shown in Figure 1b,c, respectively.

The TFLN waveguide is fabricated on an LNOI substrate with a lithium-niobate (LN) layer of 400 nm in thickness and a buried oxide (BOX) layer of 4.7 μm in thickness. It is a rib waveguide with a height of 200 nm and a width of 1 μm. To protect the TFLN waveguide and reduce its propagation loss, a top oxide (TOX) layer of 1 μm in thickness is deposited. However, the TOX layer on the DLCS needs to be removed to enhance the coupling efficiency between the DLCS and the PWB waveguide. Dry etching is used to remove the TOX on the DLCS. To avoid the risk of over-etching damaging the TFLN waveguide, the condition of under-etching is carefully controlled, leading to a thin oxide layer on the DLCS with a thickness of h.

As shown in Figure 1c, the DLCS has a tapered ridge that narrows adiabatically from an initial width of 1 μm to w_1, combined with a multi-segment strip taper terminating at a width of w_2. This design ensures adiabatic mode transformation, by which the photons transfer from the TFLN waveguide to the PWB waveguide with high efficiency. The structural parameters (w_1, w_2, and taper geometry) are optimized according to ref. [23]. The PWB waveguide, designed as a strip waveguide with a cross-section of 3×3 μm, has a bending radius r (Figure 1a) to direct the photons vertically to the SPAD.

To select a proper bending radius of the PWB waveguide, its bending loss under different bending radii (r) is simulated by a commercial photonic simulation software (Lumerical), and the result is shown in Figure 1d. It can be seen that the bending loss is less than 10^{-2} dB cm^{-1} under a radius of over 90 μm. In this work, a bending radius of 100 μm is selected to ensure that the bending loss of the PWB waveguide is negligible.

The oxide layer thickness (h) on the DLCS would impact the coupling loss between the TFLN waveguide and the PWB waveguide. It has also been simulated under different h using the Finite-difference time-domain (FDTD) method, and the result is shown in Figure 1e. It shows that the coupling loss obviously increases if h is higher than 200 nm. Considering both optical performance and fabrication condition, an oxide layer thickness of 50 nm is selected in this work, minimizing coupling loss while ensuring the under-etching condition when the TOX on the DLCS is removed.

Finally, the process of light propagation in the integration scheme is simulated by the Full-wave FDTD method under the optimized DLCS geometry, $r = 100$ μm, and $h = 50$ nm. As illustrated in Figure 1f, the fundamental quasi-TE mode (electric field polarized along the y-axis) in the TFLN waveguide is adiabatically transferred to the PWB waveguide via the DLCS. The PWB waveguide then directs light from the x-direction to the z-direction with high efficiency. A total insertion loss of 0.27 dB is achieved, showing the feasibility of the proposed hybrid integration scheme based on PWB.

2.2. Fabrication Process of the Sample

First, the TFLN photonic chip with the waveguide and the DLCS is fabricated as following process: A hard mask is fabricated by electron beam lithography (EBL) lift-off process, which is a chromium (Cr) layer of 100 nm in thickness deposited by electron beam evaporation (EBE). Defined by the hard mask, the rib waveguide and other on-chip optical circuits are fabricated by inductively coupled plasma (ICP) dry etching, and the etching depth is 200 nm. Then, using a layer of amorphous silicon (a-Si) as the mask, which is prepared by sputtering, EBL, and ICP etching, the multi-segment stripe taper (Figure 1c) is fabricated by another ICP etching process. An oxide layer (SiO_2) of 1 μm in thickness is deposited by plasma-enhanced chemical vapor deposition (PECVD) as the top cladding of the waveguide. Finally, reactive ion etching (RIE) is used to remove the oxide layer on the DLCS. The photograph of the TFLN photonic chip with the DLCS and an on-chip beam splitter (BS) is shown in **Figure 2**a. The inset is the scanning electron microscopy (SEM) picture of the DLCS.

Figure 2b shows the photograph of the InGaAs/InP SPAD chip (provided by Yunnan University). It has a round photon-sensitive area with a diameter of 25 μm. The integration process of the TFLN photonic chip and the SPAD via PWB is illustrated in Figure 2c. The TFLN photonic chip and the SPAD are mounted on two holders, respectively. The positions of the DLCS on the chip and the photon-sensitive area on the SPAD are roughly aligned by a motorized three-axis stage, with a proper height difference. The region of the DLCS and the photon-sensitive area of the SPAD is filled with negative-tone photoresist (SU-8 2025) uniformly. Pre-baking is performed at 95 °C for 60 min. Then, femtosecond laser direct writing (wavelength: 780 nm, pulse energy: 40 pJ, repetition frequency: 80 MHz) is applied to fabricate the PWB waveguide via two-photon polymerization. After post-exposure baking, the sample is immersed in acetone for a few seconds to dissolve the unexposed photoresist, leaving a freestanding polymer waveguide connecting the TFLN photonic chip and the SPAD.

Figure 2d shows the SEM picture of the PWB waveguide fabricated by this process. Its flexibility enables robust optical interconnection even under a lateral misalignment of several tens of micrometers. As shown in Figure 2d-(i), the PWB waveguide has a suspended span of over 300 μm. The details of the DLCS-PWB connection and the PWB-SPAD connection are provided in Figure 2d-(ii,iii), showing that the PWB technology supports stable and reliable optical interconnection between the two chips.

2.3. Experimental Setup

The experimental setup for characterizing the PWB-integrated SPAD is shown in **Figure 3**a. A passively mode-locked laser at 1550 nm with a pulse width of 5–10 ps and a repetition rate of 10 MHz is used as the light source. Its output light is split into two paths by a 50:50 fiber coupler (FC). In one path, the light is sent to an optical power meter (EXFO FTB-1750, ± 5% uncertainty) for power monitoring. In the other path, the light is attenuated to a single-photon level by a variable optical attenuator (VOA, EXFO FTB-3500), then the attenuated light is coupled into the TFLN photonic chip through a fiber polarization controller (FPC) and a fiber array (FA). The FPC is used to control the light polarization and ensure that it is coupled to the quasi-TE mode of the TFLN waveguide. On the TFLN photonic chip, an on-chip BS directs half of the input light to the integrated SPAD and the other half to an output port for power calibration. The SPAD is driven by a 1.25 GHz sinusoidal gating signal from a radiofrequency (RF) signal generator, synchronized to the 10 MHz laser. A custom-designed printed circuit board (PCB) combines the RF

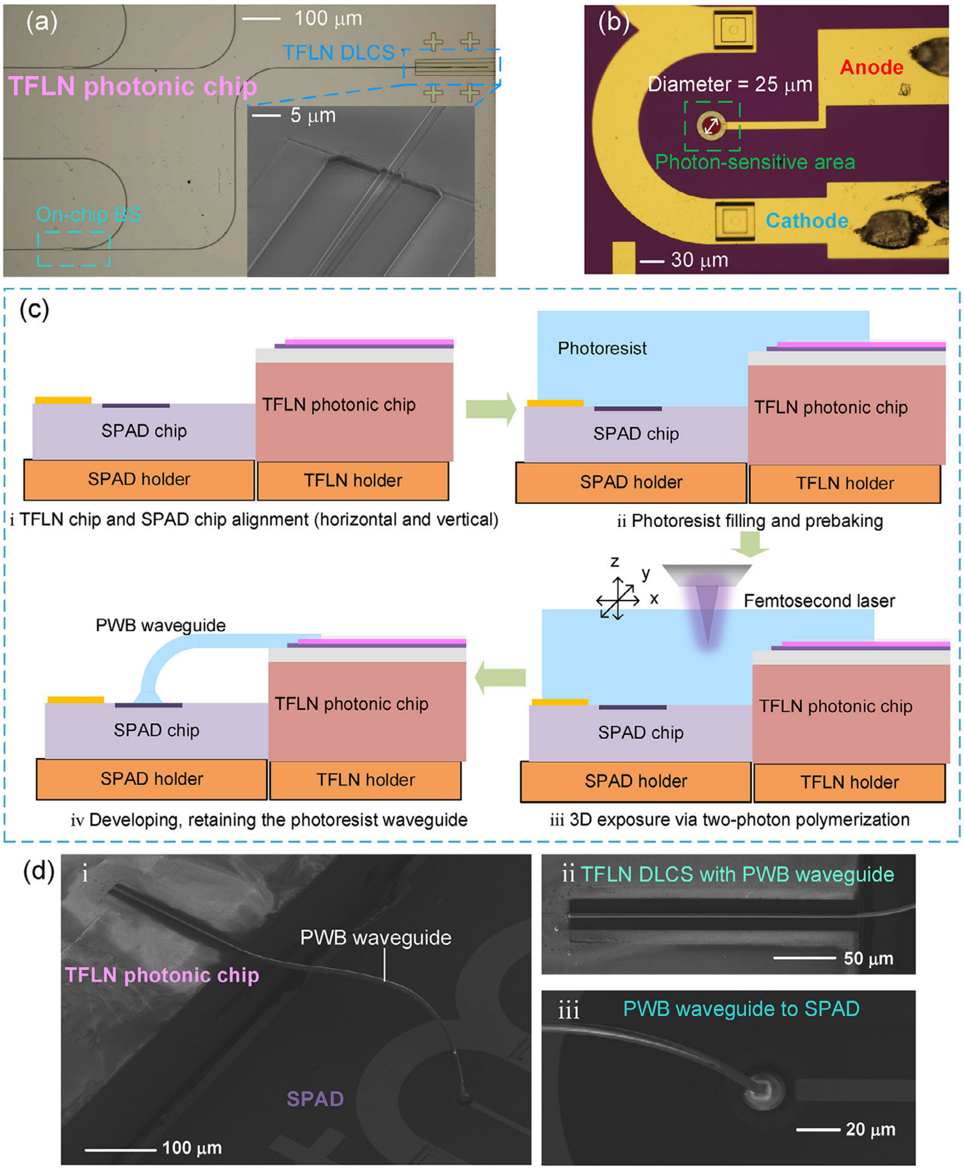

Figure 2. Fabrication process and the sample of TFLN-PWB-SPAD integration. a) Photograph of the TFLN photonic chip. Inset: SEM picture of the DLCS. b) Photograph of the InGaAs/InP SPAD chip (provided by Yunnan University). It has a round photon-sensitive area with a diameter of 25 μm. c) The process of the PWB-based hybrid integration: (i) alignment of the TFLN photonic chip and the SPAD, (ii) photoresist filling and prebaking, (iii) laser patterning, (iv) polymer waveguide development. d) SEM pictures of the PWB waveguide: (i) the PWB waveguide with a span over 300 μm, connecting the DLCS and the photon-sensitive area of the SPAD. (ii) The DLCS-PWB connection, (iii) the PWB-SPAD connection.

signal with a DC bias voltage to enable the gated operation and quenching of the SPAD. The SPAD output signal is processed by a readout circuit to extract the avalanche pulse. A thermoelectric cooler (TEC) is used to control the operating temperature of the TFLN-PWB-SPAD integration module.

The sketch of the readout circuit is illustrated in Figure 3b. The output signal of the SPAD has the contributions of the sinusoidal gating signal and the avalanche pulses. Hence, a 1.25 GHz band-stop filter is used to suppress the sinusoidal gating signal first. Then, a 2 GHz low-pass filter and an additional 1.25 GHz band-stop filter are used to eliminate residual harmonics. The filtered signal is amplified by an amplifier with a bandwidth of 6 GHz. Another 2 GHz low-pass filter is used to remove the high-frequency noise of the amplifier. The second amplifier further amplifies the signal of avalanche pulses, enabling the voltage discriminator to detect the avalanche pulses and convert them into square pulses for photon counting. Then, the square pulses are sent to a time-to-digital converter (TDC, Swabian Time Tagger Ultra) for time-correlated single-photon counting (TCSPC). The coincidence counting rate between the SPAD output and the laser synchronization signal is used to characterize the photon detection efficiency (PDE), dark count rate (DCR), and after-pulse probability (APP) of the PWB-integrated SPAD.

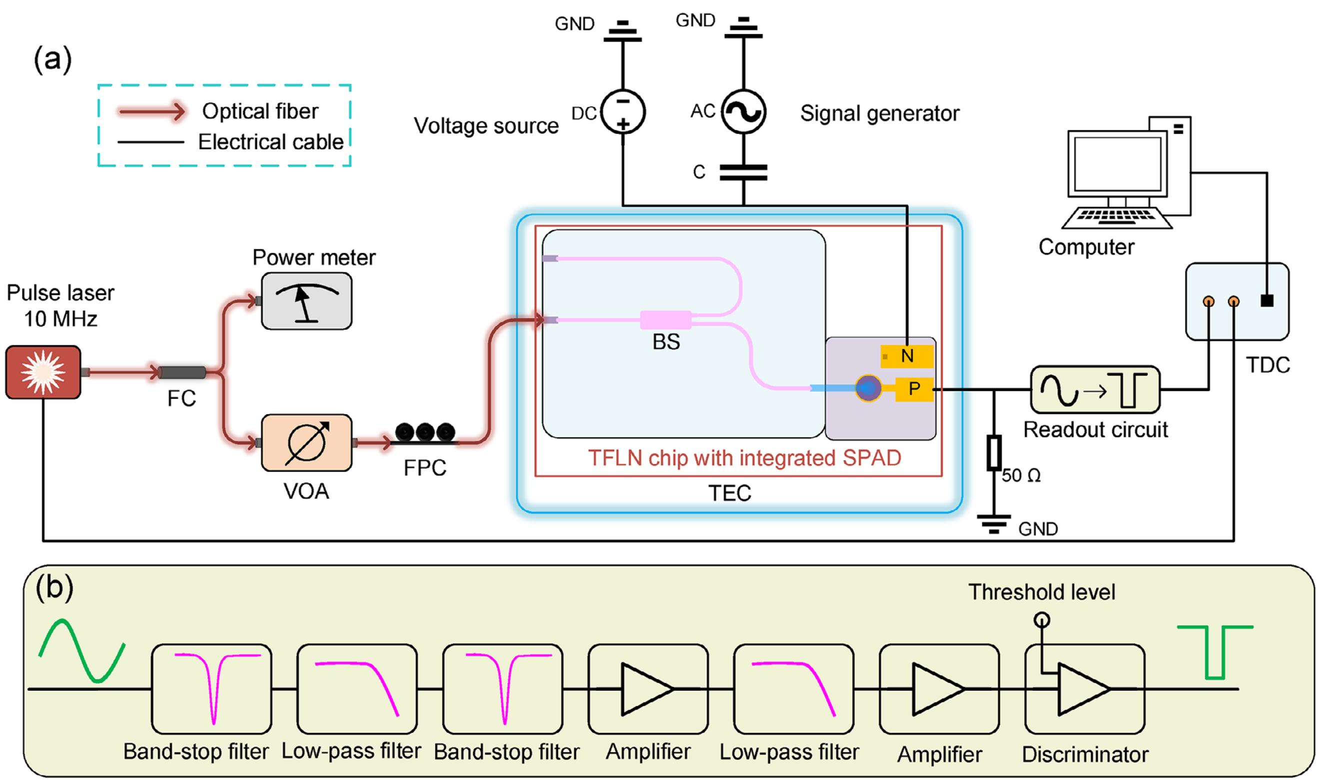

Figure 3. Experimental setup for characterizing the PWB-integrated SPAD. a) Optical and electrical configuration for SPAD performance testing under 1.25 GHz sinusoidal gated quenching. b) Sketch of the SPAD readout circuit. The band-stop (1.25 GHz) and low-pass (2 GHz) filters suppress the sinusoidal gating signal and noise, while the amplifiers boost the avalanche pulses. The voltage discriminator converts the avalanche pulses to digital pulses for counting. FC: fiber coupler; VOA: variable optical attenuator; FPC: fiber polarization controller; TDC: time-to-digital converter; BS: beam splitter.

2.4. Experimental Results

The on-chip photon detection efficiency (on-chip PDE) of the PWB-integrated SPAD is denoted by $\eta_{on\text{-}chip}$ and defined as the probability that a photon propagating in the TFLN waveguide before the DLCS is successfully coupled into the PWB waveguide and detected by the SPAD. It is determined by the coupling loss of the DLCS-PWB connection ($\eta_{DLCS\text{-}PWB}$), the propagation loss of the PWB waveguide (η_{PWB}), and the intrinsic efficiency of the SPAD (η_{SPAD}), as shown in Equation (1).

$$\eta_{on-chip} = \eta_{DLCS-PWB} \cdot \eta_{PWB} \cdot \eta_{SPAD} \tag{1}$$

In the experiment, the on-chip PDE is measured according to the following expression[24]:

$$\eta_{on-chip} = \frac{P_I - P_{NI}}{1 - e^{-\mu}} \tag{2}$$

where μ is the mean photon number per pulse in the TFLN waveguide before the DLCS, P_I and P_{NI} are counting probabilities for the illuminated gating windows and non-illuminated gating windows, respectively.

The APP of the PWB-integrated SPAD is denoted by P_{AP} and can be calculated by[25]:

$$P_{AP} = \frac{\left(P_{NI} - P_D\right) \cdot R}{P_I - P_{NI}} \tag{3}$$

where P_D is the dark count probability, measured under the condition that no light is injected into the SPAD. $R = 125$ is the ratio of the gating frequency (1.25 GHz) to the laser repetition rate (10 MHz).

The experimental results of the PWB-integrated SPAD are shown in **Figure 4**. A 1.25 GHz sinusoidal gating signal with a DC bias is applied to the SPAD. By varying the DC bias voltage (V_{bias}) on the SPAD cathode, the on-chip PDE, DCR, and APP of the SPAD are characterized at -30 °C, which is controlled by the TEC. As shown in Figure 4a, the on-chip PDE rises with increasing V_{bias}, achieves its maximum (13.8%) under $V_{bias} = 63.2$ V, then decreases due to rapidly increasing DCR (Figure 4b). The DCR shows a rapid rise when V_{bias} exceeds 63.2 V, accompanied by a sharp increase of APP larger than 10% (Figure 4c). Under the bias voltage achieving the maximum on-chip PDE, the DCR of the SPAD is $\approx 6 \times 10^{-4}$ and the APP of the SPAD is ≈3%. To characterize the time jitter of the PWB-integrated SPAD, we make the measurement of TCSPC based on the setup shown in Figure 3a. When the on-chip PDE reaches its maximum value (13.8% under $V_{bias} = 63.2$ V), the time jitter of the SPAD is ≈373 ps, which

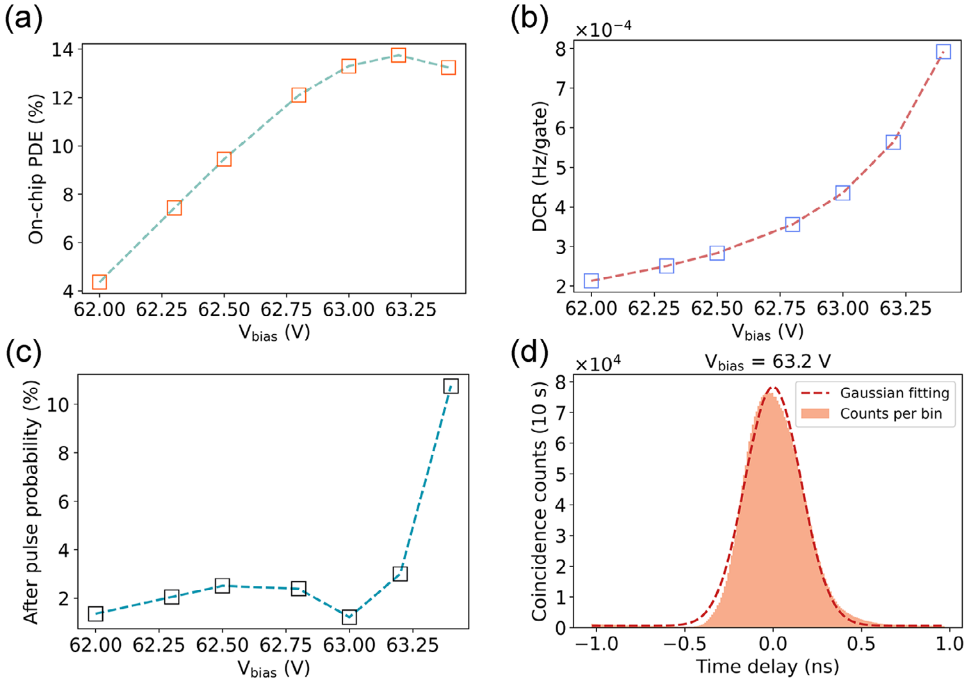

Figure 4. Performance characterization of the PWB-integrated SPAD. a) On-chip PDE, b) DCR (Hz/gate), and c) APP under increasing bias voltage (V_{bias}). d) Coincidence peak measured by TCSPC between the laser synchronization signal and single photon detection signal of the SPAD under V_{bias} = 63.2 V (Maximum on-chip PDE is achieved).

is indicated by the full-width-at-half-maximum (FWHM) of the measured coincidence peak shown in Figure 4d. It can be seen that the PWB-integrated SPAD shows reasonable performance on single-photon detection. To show the possible impact of the PWB fabrication process on the SPAD, the DCRs of a SPAD chip before and after the PWB fabrication process are measured, and the results are shown in the Supporting Information. Together with the results shown in Figure 4, it can be seen that the PWB fabrication process does not introduce obvious performance degeneration on SPADs.

3. Discussion

In the experiment, the calibration of the mean photon number per pulse in the TFLN waveguide before the DLCS is crucial for the measurement of the on-chip PDE. The power of the pulsed light before the VOA in the setup is monitored by the power meter. It is attenuated by the VOA and the optical losses of the TFLN photonic chip, including the coupling loss between the fiber and the edge coupler, the splitting loss of the on-chip BS, and the propagation loss of the TFLN waveguide. The attenuation introduced by the VOA is 54 dB. The TFLN photonic chip has an on-chip BS. One output port of the on-chip BS is connected to the DLCS, interfacing with the PWB waveguide, and the other output port is connected to an edge coupler, which is used as a monitor port for optical loss calibration. Before the SPAD characterization, the total insertion loss between the input port and the monitor port of the TFLN photonic chip is measured to be 12.3 dB. Then, the insertion loss of a reference short waveguide with two edge couplers is measured to be 8 dB, showing that the coupling loss between fiber and this TFLN photonic chip is ≈4 dB per facet. Hence, the attenuation introduced by the optical losses of the chip can be estimated to be 8.3 dB. As a result, the total attenuation between the point before the VOA and that before the DLCS is 62.3 dB. According to the monitored light power before the VOA and the total light attenuation, the average photon number per pulse before the DLCS can be determined, which is $\mu \approx 0.25$. After the calibration, the performance is characterized experimentally, and the on-chip PDE is calculated according to Equation (2).

It is obvious that the hybrid integration scheme proposed in this work could be applied to other types of photonic chips, as long as the on-chip coupling structures for the PWB waveguide are appropriately designed. We compare the SPAD performance of this work with those of two recent works about the integration of InGaAs/InP SPADs on silicon photonic chips, as shown in **Table 1**. In the work of ref. [26], a heterogeneous integration scheme based on buffer-layer-based material bonding and etching is demonstrated. In the work of ref. [27], the hybrid integration is achieved based on flip-chip bonding. In both works, waveguide grating couplers are used to couple the light vertically to the SPADs. Our work demonstrates the hybrid integration of InGaAs/InP SPADs and TFLN photonic chips via PWB. The PWB-integrated SPAD achieves an on-chip PDE of 13.8%, much higher than those in the two previous works. The flexibility of the PWB waveguide relaxes the requirement of optical alignment between the on-chip waveguide and the SPAD. The PWB technology also supports parallel integration of multiple SPADs on a photonic chip. Besides, the scheme in our work uses off-the-shelf SPAD chips, even the pre-selected high-performance ones, to achieve the hybrid integration, ensuring its wide applicability with high performance.

Table 1. Integration schemes of InGaAs/InP SPADs on photonic chips.

Reference	On-chip PDE [%]	DCR [Hz/gate]	Integration scheme	Quenching circuit	Temperature [K]
[26]	≈6	2.4×10^{-1}	III-V material transfer via buffer layer onto Si photonic chip, followed by SPAD fabrication	1 kHz square-wave gating (20 ns gate width)	220
[27]	5–6	10^{-5}–10^{-4}	Flip-chip bonding with grating couplers	500 MHz sinusoidal gating (≈1 ns gate width)	283
This work	13.8	10^{-4}	Photonic wire bonding (PWB)	1.25 GHz sinusoidal gating (≈400 ps gate width)	243

It is worth noting that the performance of the PWB-integrated SPAD has the potential to be further improved. In this work, additional losses arise from the coupling between the DLCS and the PWB waveguide, as well as the defects in the PWB waveguide. The fabrication process of the DLCS and the TFLN waveguide could be improved. For example, the chemical polishing process could be used to reduce the sidewall roughness of the waveguide, thereby reducing the waveguide loss and enhancing the coupling efficiency.[28] The exposure parameters of the femtosecond laser (pulse energy, scan speed) in the fabrication process of the PWB waveguide could also be optimized to reduce the defects, such as localized polymer agglomerations and surface irregularities (Figure 2d-(iii)). The DCR performance could be improved through some optimizations in the quenching circuit. For example, active dead time could be implemented to suppress DCR by increasing non-avalanche time.[29] The measured time jitter (≈370 ps) is limited by the 2 GHz low-pass filters in the readout circuit, which truncate the high-frequency components of the avalanche signal. Adopting ultra-narrowband interferometric band-stop filters could preserve signal bandwidth while rejecting sinusoidal gating signal, potentially reducing jitter to < 200 ps.[30,31]

4. Conclusion

In this work, a hybrid integration scheme of InGaAs/InP SPADs and TFLN photonic chips via PWB is proposed and demonstrated. A suspended polymer waveguide with a span over 300 μm is fabricated to guide photons from the DLCS at the end of the TFLN waveguide to the photon-sensitive area of the SPAD. The PWB-integrated SPAD achieves an on-chip PDE of 13.8% at −30 °C, with a DCR of $\approx 6 \times 10^{-4}$ Hz/gate, an APP of ≈3%, and a time jitter of ≈370 ps. The flexibility of the PWB waveguides enables robust optical connection and highly relaxes the requirement of optical alignment, making it a promising solution for hybrid integration on various quantum photonic chips. The PWB technology also supports multi-channel optical connection; hence, it can also be used to integrate single-photon detector arrays on photonic chips. Further improvements in on-chip PDE, DCR, and APP can be expected by optimizing the fabrication processes of the DLCS and PWB waveguides and utilizing improved quenching and readout circuits. This hybrid integration scheme provides a convenient approach to achieve compact, cost-effective, and scalable single-photon detection on the TFLN platform. It has great potential to be applied in receivers of quantum communication and weak-light sensing, such as single-photon counting OTDR and chip-scale LiDAR.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

hybrid integration, integrated quantum photonic chip, photonic wire bonding, single-photon avalanche diode, thin-film lithium niobate

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